A Digital Clock Re-Timing Circuit For On-Chip Source-Synchronous Serial Links

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Summary

A new all-digital circuit scheme for clock and data re-timing functions for on-chip high-speed source synchronous data communications, such as in burst-mode data transmission over a network-on-chip is introduced. The new technique is non-PLL-based and is capable of retiming the output clock with the received data within one data transition. Being fully digital makes its area much smaller than conventional circuitry. It can also be described by any hardware description language, simulated, and synthesized into any digital process. This enables it to be ported from one technology to another and support system on a chip (SOC) designs. The design concept is demonstrated with T-Spice?? simulations using a 0.13??m digital CMOS technology.